## REMARKS

The present response is intended to be fully responsive to all points of rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Claims 1-35 are pending in this case. The amendment filed November 30, 2007 is objected to. Claims 7, 12-13, 2-, 22-23, 32, 34-35 are objected to. Claim 7 is rejected under 35 U.S.C. § 112, second paragraph. Claims 24-26, 31 have been rejected under 35 U.S.C. § 102(e). Claims 1-23, 27-30, 32-35 have been rejected under 35 U.S.C. § 103(a). Independent claims 1, 14, 24 and dependent claims 4-5, 7, 9-10, 12-13, 15, 17-18, 20, 22-23, 32, 34-35 have been amended. New claims 36-37 have been added.

### Telephonic Interview

Applicant wishes to thank the Examiner for granting a telephonic interview on march 15, 2008. The interview participants included Examiner Ramnandan P. Singh, Howard Zaretsky (Applicant's representative) and Oren Eliezer (Applicant).

### Response to Response to Amendment

The Examiner objected to the amendment filed November 30, 2007 under 35 U.S.C. § 132(a) because it introduces new matter into the disclosure. Paragraphs [0007], [0011] and [0012] have been amended in accordance with the suggestions of the Examiner.

### Response to Objection to the Claims

Claims 7, 12-13, 20, 22-23, 32, 34-35 are objected to because of informalities, e.g., the limitation "adapted to". Applicant has amended claims 7, 12-13, 20, 22-23, 32, 34-35 accordingly.

**Response to 35 U.S.C. § 112, Second Paragraph Rejections**

The Examiner rejected claim 7 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Specifically, the Examiner has pointed out that the term 'substantially' in claim 7 is a relative term which renders the claim indefinite.

Amended claim 7 now features language which makes it clear what the subject matter is that the Applicant regards as the invention. Applicant believes that amended claim 7 overcomes the Examiner's rejection based on § 112, second paragraph grounds. The Examiner is respectfully requested to withdraw the § 112, second paragraph rejection.

**Response to 35 U.S.C. § 102(e) Rejections**

The Examiner rejected claims 24-26, 31 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,963,629 ("Boerstler et al."). Applicant respectfully submits that the prior art fails to disclose or suggest at least means for using phase error samples taken from an internal PLL to test an oscillator that is part of a transmitter, wherein the phase error samples correspond to the phase modulation noise of the oscillator. Therefore, Applicant respectfully traverses the rejections and request favorable reconsideration.

Boerstler et al. teaches a reference signal and a voltage controlled oscillator (VCO) output are compared for relative phase and frequency differences. A lead error signal is generated if the reference signal leads the VCO output and a lag error signal is generated if the reference signal lags the VCO output the lead and lag error may result from a combination for phase and frequency differences between the reference signal and the VCO output. A time window is used to sample the polarity of the lead and lag error signals by incrementing and

decrementing a phase error signal. If the phase error signal reaches a threshold value within the time window, a Reset Delta pulse is generated and if the phase error signals does not reach the maximum delta value within the time window a Reset Total pulse is generated. A variable first gain signal is increased on each Reset Delta pulse and decreased on each Reset Total pulse and limited to a value between predetermined maximum and minimum values. The first gain signal is multiplied by a Pump current increment and added to a minimum Pump current to generate a variable Pump current. A variable second gain signal proportional to the time the reference signal leads and lags the VCO signal multiplies the Pump current. The amplified Pump current is summed with an integral of the amplified Pump current to generate a control signal. The control signal is applied to the VCO and determines the frequency of the VCO output.

While continuing to traverse the Examiner's rejections, Applicant, in order to expedite the prosecution, has chosen to clarify and emphasize the crucial distinctions between the present invention and the devices of the patents cited by the Examiner. Specifically, claim 1 has been amended to include an apparatus for testing an oscillator in a transmitter, comprising first means for measuring a phase error signal within a phase locked loop in the transmitter, wherein the phase error signal corresponds to the phase modulation noise of the oscillator, second means for comparing a plurality of phase error signal samples over a period of time to a threshold and generating an exception event each time a phase error signal sample exceeds the threshold, and generating a failure indication if the number of exception events exceeds a criteria and generating a pass indication otherwise.

It is submitted that the mechanism of Boerstler et al. is intended for use in a receiver for the purposes of **normal receiver demodulation**. The mechanism of Boerstler et al. is a different solution to a different problem. The problem being that of reducing the time required for a

microprocessor or other circuit to "wake up" after shutting off the device's clock generator circuit for power reduction purposes. The time needed to wake-up may be excessive since the PLL clock source may require a long period of time to achieve the desired steady-state conditions. Thus, Boerstler et al. provides an adaptive PLL (as described supra) that has fast acquisition time and low jitter while requiring simple hardware to implement.

In contrast, the present invention is a mechanism for **testing an oscillator** that is part of a PLL circuit in a transmitter (or receiver). The mechanism effectively **estimates the phase modulation noise** of the oscillator by **observing the phase error signal (PHE)** inside the PLL circuit as opposed to the high frequency RF signal at the output of the transmitter. The phase noise estimation mechanism is used in the transmitter (or receiver), **not** for normal transmit or receive operations, **but rather for testing or performance monitoring purposes**. The mechanism is intended for testing purposes where it is required to ensure that the transmitter (or receiver) of a radio comply with the modulation quality or phase noise requirements of a communications standard, such as Bluetooth or GSM. The testing circuit taught by the present invention may be left out without any consequence to the regular operation of the PLL or transmitter.

See Paragraphs [0038] and [0039] for an analysis of the theory as to why the statistics of the deviation errors in the RF output can be estimated through measurements of the phase error signal *PHE* generated internally in the PLL.

In is submitted that the mechanism of Boerstler et al. generates phase error signal lead and lag signals and the phase error signal. The circuit of Boerstler et al. uses UP/DOWN signals to manipulate the phase error signal to compensate for up and down transitions in the phase error

due to jitter on the reference and VCO output clocks. Thus, Boerstler et al. provides PLL loop circuitry that is used in the generation of the PLL output signal.

In contrast, the mechanism of the present invention is ancillary to the operation of the PLL and does not effect its normal operation. The mechanism is a test scheme that is capable of testing the oscillator within a phase-locked loop of a transmitter or receiver. The mechanism does not interfere with the normal operation of the PLL.

Modulation inaccuracies and phase noise on the oscillator that is used to generate the carrier frequency (in a transmitter for example) translate, after frequency demodulation at the receiver, to distortion and additive baseband noise, which could degrade the receiver's performance. For this reason, transmitters must be tested for compliance against the defined modulation quality criteria as specified by the relevant standard (e.g., Bluetooth, GSM, etc.), which specifies the permitted limits on the amount of distortion and noise in the TX circuitry.

In a two-point modulation injection transmitter, such as described in the present invention, assuming a stable reference crystal (e.g., DCXO), the phase error at the output of the phase detector in the PLL in the transmitter, corresponds to the undesirable portion (i.e. noise and modulation errors) of the modulation. Further, since the modulation errors and noise at the RF output (within a certain bandwidth) correspond to the phase error, the invention estimates their statistics via measurements of the phase error signal within the PLL. The mechanism of the present invention serves to determine compliance of the device with the relevant specifications **without** requiring statistical estimations and calculations of high complexity. Thus, the invention **eliminates** the requirement of performing complex calculations of the variance of the noise (which represents both its power and its probability to exceed the value for which an exception event would occur). Calculating the variance normally entails computing the mean of

the squares of differences between the sampled values and their average, which is very costly in terms of required processing resources.

Instead, the mechanism of the present inventions **estimates** the level of noise by **counting the number of times** (called exceptions) the normalized phase error crosses a threshold within a predefined period of time. The value of the count corresponds to the noise power via the distribution function of the noise. If the count exceeds a predefined (software configurable) maximum, the device under test fails, otherwise it passes. The maximum number of exceptions permitted is set to correspond to the modulation quality requirement of the particular standard. Thus, the invention trades complex computations of variance and other statistics on the phase error signal for a relatively simple thresholding and counting mechanism that is much easier and cheaper to implement. These features are neither taught nor suggested by the Boerstler et al. reference cited by the Examiner.

Applicant has reviewed the cited art and respectfully submits that the art fails to disclose or suggest the Applicant's claimed invention, and fails to teach each and every element and limitation of the claims rejected herein. Therefore Applicant respectfully traverses the rejections and requests favorable reconsideration.

It is believed that amended independent claim 24 overcome the Examiner's § 102(e) rejection based on the Boerstler et al. reference. In addition, it is believed that amended dependent claims 25-26, 31 dependent on claim 24 also overcome the Examiner's rejection based on § 102(e) grounds. The Examiner is respectfully requested to withdraw the rejection based on § 102(e).

**Response to 35 U.S.C. § 103(a) Rejections**

Claims 1, 3-6, 8, 12-14, 16-19, 22-23:

The Examiner rejected claims 1, 3-6, 8, 12-14, 16-19, 22-23 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,963,629 ("Boerstler et al."). To reject the claims as obvious under 35 U.S.C. §103(a) there must be some suggestion or motivation, either in the references themselves or in the prior art, to modify or combine teachings. Furthermore, the prior art references must teach all the claimed limitations. Applicant has reviewed the cited art and respectfully submits that the art fails to disclose or suggest the Applicant's claimed invention, and fails to teach each and every element and limitation of the claims rejected herein. Specifically, Applicant respectfully submits that the prior art fails to disclose or suggest at least the step of using phase error samples taken from an internal PLL to test an oscillator that is part of a transmitter or receiver, wherein the phase error samples correspond to the phase noise of the oscillator. Therefore, Applicant respectfully traverses the rejections and requests favorable reconsideration.

While continuing to traverse the Examiner's rejections, Applicant, in order to expedite the prosecution, has chosen to clarify and emphasize the crucial distinctions between the present invention and the devices of the patents cited by the Examiner. Specifically, representative claim 1 has been amended to include a method of **testing an oscillator** in a phase locked loop, said method comprising the steps of averaging phase error samples produced by said phase locked loop, wherein said phase error samples correspond to the phase modulation noise of said oscillator, subtracting said average from a current phase error sample to yield a normalized phase error, generating an exception event if said normalized phase error exceeds a threshold, thereby indicating that the level of oscillator phase noise is not acceptable, and repeating said steps of

averaging, subtracting and generating over a period of time and outputting a failure indication if the number of exception events exceeds a maximum criteria and a pass indication otherwise.

As stated supra, it is submitted that the mechanism of Boerstler et al. is intended for use in a receiver for the purposes of **normal receiver demodulation**. The mechanism of Boerstler et al. is a different solution to a different problem. The problem being that of reducing the time required for a microprocessor or other circuit to "wake up" after shutting off the device's clock generator circuit for power reduction purposes. The time needed to wake-up may be excessive since the PLL clock source may require a long period of time to achieve the desired steady-state conditions. Thus, Boerstler et al. provides an adaptive PLL (as described supra) that has fast acquisition time and low jitter while requiring simple hardware to implement.

In contrast, the present invention is a mechanism for **testing an oscillator** that is part of a PLL circuit in a transmitter (or receiver). The mechanism effectively **estimates the phase modulation noise** of the oscillator by **observing the phase error signal (PHE)** inside the PLL circuit as opposed to the high frequency RF signal at the output of the transmitter. The phase noise estimation mechanism is used in the transmitter (or receiver), **not** for normal transmit or receive operations, **but rather for testing or performance monitoring purposes**. The mechanism is intended for testing purposes where it is required to ensure that the transmitter (or receiver) of a radio comply with the modulation quality or phase noise requirements of a communications standard, such as Bluetooth or GSM. The testing circuit taught by the present invention may be left out without any consequence to the regular operation of the PLL or transmitter.

In is submitted that the mechanism of Boerstler et al. generates phase error signal lead and lag signals and the phase error signal. The circuit of Boerstler et al. uses UP/DOWN signals

to manipulate the phase error signal to compensate for up and down transitions in the phase error due to jitter on the reference and VCO output clocks. Thus, Boerstler et al. provides PLL loop circuitry that is used in the generation of the PLL output signal.

In contrast, the mechanism of the present invention is ancillary to the operation of the PLL and does not effect its normal operation. The mechanism is a test scheme that is capable of testing the oscillator within the transmitter. The mechanism does not interfere with the normal operation of the PLL.

Applicant respectfully submits that the Examiner has failed to show that one of ordinary skill in the art would have been motivated to modify Boerstler et al. to arrive at the claimed invention because there is no suggestion made by Boerstler et al. to perform **testing of the oscillator** (i.e. **perform phase modulation noise measurements**) in a transmitter by **counting** the number of times the normalized phase error within a PLL crosses a **threshold**.

Applicant submits that Examiner has not made a *prima facie* case of obviousness. The teaching or suggestion to make the claimed combination must be found in the prior art, not in Applicant's disclosure (*In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Applicant therefore submits that independent claims 1, 14 are allowable and requests favorable reconsideration. Further, since Boerstler et al. does not anticipate or suggest claims 1, 14 as discussed above, then dependent claims 3-6, 8, 12-13, 16-19, 22-23 are allowable as well. The Applicant respectfully traverses the objections of claims 1, 3-6, 8, 12-14, 16-19, 22-23 and submits that the presently claimed invention is patently distinct over Boerstler et al. The Examiner is respectfully requested to withdraw the rejection based on § 103(a).

Claims 2 and 15:

The Examiner rejected claims 2 and 15 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,963,629 ("Boerstler et al.") in view of U.S. Patent No. 6,603,821 ("Doi").

Doi teaches a power calculator calculates the power of an input signal in accordance with a component of an input received signal. A comparator asserts an unmodulated signal detection signal when the power calculated by the power calculator exceeds a prescribed threshold. A maximum value detector detects the maximum power of the input received signal in accordance with the assertion of the unmodulated signal detection signal and generates non-modulated signal position instruction information with a maximum value detection signal, and a frequency error calculator calculates an error of a carrier frequency on the basis of the received signal corresponding to the maximum power. The frequency error is calculated only with a non-modulated signal, whereby the frequency error can be correctly calculated and the non-modulated signal position can also be correctly detected.

In light of the amendments and arguments presented above in connection with independent claims 1 and 14, Applicant believes that dependent claims 2 and 15 overcome the Examiner's § 103(a) rejection based on the Boerstler et al. and Doi references. The Examiner is respectfully requested to withdraw the rejection based on § 103(a).

Claims 7, 20-21:

The Examiner rejected claims 7, 20-21 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,963,629 ("Boerstler et al.") in view of U.S. Patent No. 6,665,339 ("Adams et al.").

Adams et al. teaches a monolithic transceiver integrated circuit that includes a substrate, a transmitter subsystem of one or more subcircuits on the substrate, and a receiver subsystem of

one or more, subcircuits on the substrate. Also included is a bias current supply coupled to the receiver and transmitter subsystems to provide bias current. The bias current supply includes a first bias circuit on the substrate coupled to, and to supply bias current to, a first subcircuit of the transmitter subsystem. The first bias circuit includes a first current modulator having a first switch input to indicate that the bias current is to start or stop being supplied to the first subcircuit. The first current modulator is to control the rate of change of supplied bias current in response to the first switch input. The first subcircuit may be a power amplifier. The control of the rate of change reduces oscillator pull in at least one oscillator included in the integrated circuit.

In light of the amendments and arguments presented above in connection with independent claims 1 and 14, Applicant believes that dependent claims 7, 20-21 overcome the Examiner's § 103(a) rejection based on the Boerstler et al. and Adams et al. references. The Examiner is respectfully requested to withdraw the rejection based on § 103(a).

Claims 9-10:

The Examiner rejected claims 9-10 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,963,629 ("Boerstler et al.").

In light of the amendments and arguments presented above in connection with independent claim 1, Applicant believes that dependent claims 9-10 overcome the Examiner's § 103(a) rejection based on the Boerstler et al. reference. The Examiner is respectfully requested to withdraw the rejection based on § 103(a).

Claim 11:

The Examiner rejected claim 11 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,963,629 ("Boerstler et al.") in view of U.S. Patent No. 5,883,930 ("Fukushi et al.").

Fukushi et al. teaches, in a DPLL circuit used in a receiver for radio data communication employing the GMSK modulation system, a data latch circuit 23 and subtractor 24 find the phase information difference for each symbol from the incoming phase data. A modulation component removal circuit 25 removes the modulation component from the phase information difference. A frequency error calculating circuit 26 integrates the phase information difference over an interval of n symbols, multiplies this integrated value by 1/n, and takes the result as the mean frequency error value for the interval of n symbols, and then outputs this to loop filter 32. A phase error calculating circuit 27 further integrates over an interval of n symbols the integrated value from the frequency error calculating circuit, and multiplies the result by 2/n. Adder 28 adds an initial phase latched by a data latch circuit 22 to the output of the phase error calculating circuit, and outputs the result to NCO 33 as the phase error value. Operation of loop unit 36 is commenced with a timing that is preset by the mean frequency error value and phase error value.

In light of the amendments and arguments presented above in connection with independent claim 1, Applicant believes that dependent claim 11 overcomes the Examiner's § 103(a) rejection based on the Boerstler et al. and Fukushi et al. references. The Examiner is respectfully requested to withdraw the rejection based on § 103(a).

Claims 27-20, 32-35:

The Examiner rejected claims 27-20, 32-35 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,963,629 ("Boerstler et al.").

In light of the amendments and arguments presented above in connection with independent claim 1, Applicant believes that dependent claims 27-20, 32-35 overcome the Examiner's § 103(a) rejection based on the Boerstler et al. reference. The Examiner is respectfully requested to withdraw the rejection based on § 103(a).

**Conclusion**

In view of the above amendments and remarks, it is respectfully submitted that independent claims 1, 14, 24, 36 and hence dependent claims 2-13, 15-23, 25-35, 37 are now in condition for allowance. Prompt notice of allowance is respectfully solicited.

In light of the Amendments and the arguments set forth above, Applicant earnestly believes that they are entitled to a letters patent, and respectively solicit the Examiner to expedite prosecution of this patent applications to issuance. Should the Examiner have any questions, the Examiner is encouraged to telephone the undersigned.

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Respectfully submitted,

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